Amendments to the Specification

Please amend the following paragraphs as specified.

- Please amend the paragraph beginning on page 2, line 4, as follows:

C1

Thin oxides that allow[s] direct tunneling current behave quite differently than thicker oxides, which exhibit Fowler-Nordheim tunneling. Rupturing thin oxide requires consideration for pulse width duration and amplitude to limit power through the gate oxide to produce reliable, low resistance anti-fuse.

- Please amend the paragraph beginning on page 2, line 8, as follows:

C2

Rupturing the gate oxide is a technique used to program a non-volatile memory array. U.S. Patent no. 6,044,012 discloses a technique for rupturing the gate oxide, but the oxide is about 40Å to 70Å thick. The probability of direct tunneling, rather than Fowler-Nordheim tunneling, of gate current through an oxide of this thickness is extremely low. Also, the voltage required to rupture the oxide is substantially higher and requires a charge pump circuit. The ['012] '012 patent does not disclose final programmed resistance, but such is believed to be in the high kilo (K) ohms range.

- Please amend the paragraph beginning on page 3, line 14, as follows:

C3

In one embodiment, the anti-fuse transistor is enclosed in a ~~deep-Nwell~~ deep N-well structure, which allows the surrounding ~~deep-Nwell~~ deep N-well to be biased at a different voltage to isolate the memory cell. In this embodiment, the gate can be programmed at a lower voltage than without a ~~deep-Nwell~~ deep N-well enclosure.

- Please amend the paragraph beginning on page 3, line 18, as follows:

C4

In another embodiment, the state of the anti-fuse transistor is programmed through a 5-volt tolerant circuitry and read through a 1.2-volt sensing circuit.

- Please amend the paragraph beginning on page 4, line 12, as follows:

C5

FIG. 4 illustrates another embodiment using 5-volt tolerant switches.

- Please amend the paragraph beginning on page 4, line 17, as follows:

C6

Finally, FIG. 7 illustrates a plot of the final (after programming) anti-fuse resistance ~~verses~~ versus applied power, according to the present invention.

- Please amend the paragraph beginning on page 5, line 6, as follows:

C7

According to the present invention, the physical current used to rupture (also referred to as "breakdown") an oxide is dominated by a different mechanism than in prior art anti-fuses fabricated according to 0.35μm and 0.18μm process technologies. In the present invention, the oxide rupture can be more controlled and the final programmed resistance is much lower ~~that~~ than conventional devices. A smaller variance on programmed resistance allows a more compact circuit design to determine the state of the memory cell. Moreover, the lower voltage required to rupture the anti-fuse oxide means no charge pump circuitry is required, thus making a simpler memory array design and smaller circuit area requirement.

- Please amend the paragraph beginning on page 6, line 3, as follows:

C8

FIG. 2 illustrates [a] an example schematic diagram of an embodiment corresponding to FIG. 1. The storage cell 102 comprises a resistive load (Rload) 202, a diode 204, a write switch 206, and two read switches 208 and 210. Rload 202 is an ideal representation of an anti-fuse, comprising a capacitor or MOS transistor configured as a capacitor. In the latter instance, the source and drain of the transistor are coupled together to form one plate of the capacitor. The other plate is formed by the transistor gate, and the plates are separated by a gate oxide. The gate oxide layer is approximately 20Å thick, which can be achieved with 0.13μm or less process technology. This thickness is chosen so that the gate can be ruptured by direct tunneling gate current, rather than Fowler-Nordheim tunneling.

- Please amend the paragraph beginning on page 6, line 18, as follows:

C9

Write circuit 104 comprises a read switch 212 and a write switch 214 coupled in series between zero (i.e., ground) and negative 3.5-volt supplies. Current bias and voltage clamp circuit 108 comprises a current source 216 and a 1.2-volt clamp circuit 218 to provide a 2.5-volt supply to a node labeled "vload" of the storage cell 102. The current source 216 and a 1.2-volt clamp circuit 218 are coupled to a node, which in turn is coupled to read switch 208 via a connection labeled "ifeed".

- Please amend the paragraph beginning on page 6, line 25, as follows:

C10

Rload is coupled between the vload node and switches 212 and 214 via a connection labeled "n3v5out" (negative 3.5-volt out). Closing of write switches 206 and 214, while read switches 208, 210 and 212 remain open, permits sufficient current to flow through the

C10

vload node to rupture the anti-fuse. Once programmed in this manner, the anti-fuse can be read by read circuit 106. In this arrangement, write switch 206 must have a voltage tolerance higher than that of the anti-fuse. To achieve this higher voltage tolerance, the switches, including write switch 206, are formed with thicker gate oxide layers (e.g., 50-70 [μm] Å).

- Please amend the paragraph beginning on page 7, line 16, as follows:

C11

FIG. 3 illustrates a deep N-well MOSFET used to implement the anti-fuse of the storage cell, according to an embodiment of the present invention. The deep N-well is shown at 302. Coupling of source 304 and drain 306 is shown at the n3v5out connection. The gate is [couple] coupled to vload. This low voltage CMOS anti-fuse transistor is programmed by controlled pulses of electrical current with fixed amplitude to rupture its gate oxide. The electrical power through the gate oxide cannot exceed a certain voltage and duration as to avoid creating a void in the gate oxide. The advantage of the deep N-well is to isolate the memory cell and allow biasing of the well, source and drain to ~~-3.5volts~~ -3.5 volts when write switch 214 is closed. When write switch 206 is closed, ~~2.5volts~~ 2.5 volts is applied to the gate through the vload, thus effectively creating a 6-volt voltage difference across the gate oxide to rupture it. When the gate oxide is destroyed, a conductive path is formed between the gate electrode and the source/drain regions of the anti-fuse transistor. This resistance, under controlled electrical pulses, will be in the hundreds of ohms range or less, which is 4 orders of magnitude lower than the resistance prior to programming. To apply the high programming voltage across the gate oxide of the anti-fuse transistor, the drain and source regions of the anti-fuse transistor are connected to ground, and a programming voltage is applied to the gate of the anti-fuse transistor as described above.

- Please amend the paragraph beginning on page 8, line 5, as follows:

C12

FIG. 4 illustrates another embodiment in which no deep N-well transistor is used. The transistor's gate (shown as capacitor 402) is tied to a 1.2±volt sensing circuit 404 and a 5±volt tolerant switch 406. The 5±volt tolerant switch 406 is constructed from Input/Output MOS devices having a thicker gate oxide. An example 5±volt tolerant switch that can be used to implement this alternative embodiment of the present invention is described in "A High-Voltage Output Buffer Fabricated on a 2V CMOS Technology", by L.T. Clark, 1999 Symposium on VLSI Circuits Digest of [technical] Technical Papers (June 1999). These thicker gate oxide devices are connected to a resistor 408, whose other end is tied to the 5± volt supply. By appropriate switching, as would become apparent to a person skilled in the relevant art based on the above description of the first embodiment, the oxide is ruptured to program the anti-fuse.

- Please amend the paragraph beginning on page 8, line 24, as follows:

C13

FIGs. 6A and 6B show example data resulting from programming the anti-fuse transistors using about 5 volts and reading its resistance by applying ~~0.1volts~~ 0.1 volts on the gate electrode with the grounded source/drain regions. The tight distribution of the programmed anti-fuse resistance makes the determination of its state quite easy. The 5±volt programming supply can be from the system power bus, which eliminates the need to integrate charge pump circuitry on the same chip. Data for gate dimensions of 10x10μm ~~verses~~ versus 50x2μm are illustrated. These geometries are provided by way of example and not limitation. Other geometries within the scope of the invention are contemplated by the inventors.

- Please amend the paragraph beginning on page 9, line 3, as follows:

C14

Finally, FIG. 7 illustrates a plot of the final (after programming) anti-fuse resistance ~~verses~~ versus applied power. The power is defined as Power= FuseV * I compliance * Time, as was applied by an HP4156b (Hewlett-Packard Company, Palo Alto, CA). The HP4156b is a precision semiconductor parameter analyzer used to vary three parameters for testing purposes: voltage, time duration and current compliance. HP4156b output voltage for the time duration specified and the clamp current (output to no more ~~that~~ than the current compliance specified)[,] when current starts to flow through the oxide layer is illustrated.

- Please amend the paragraph beginning on page 10, line 5, as follows:

C15

The present invention may be implemented with various changes and substitutions to the illustrated embodiments. For example, the present invention may be implemented on substrates comprised of materials other ~~that~~ than silicon, such as, for example, gallium arsenide or sapphire.

Please amend the abstract as follows (on the following, separate page):

System and Method for One-Time Programmed Memory Through Direct-Tunneling Oxide Breakdown

C16

Abstract

A one-time ~~programing~~ programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, having a capacitor, or transistor configured as a capacitor, with an oxide layer capable of passing direct gate tunneling current, and a switch having a voltage tolerance higher than that of the capacitor/transistor, wherein the capacitor/transistor is one-time programmable as an anti-fuse by application of a voltage across the oxide layer via the switch to cause direct gate tunneling current to thereby rupture the oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.